

## WEST Search History

[Hide Items](#) | [Restore](#) | [Clear](#) | [Cancel](#)

DATE: Sunday, September 18, 2005

Hide?	<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<input type="checkbox"/>	L17	L16 not L14	190
<input type="checkbox"/>	L16	(gate with width) same (photolithograph\$2 or lithograph\$2) and ((pattern or mask) with overlap\$4)	201
<input type="checkbox"/>	L15	(gate with width) same (photolithograph\$2 or lithograph\$2) and ((pattern or mask) with overlap\$4)	96
<input type="checkbox"/>	L14	L13 and (limit\$7 with (wavelength with CD or width or dimension))	300
<input type="checkbox"/>	L13	L12 or L9 or L4	775
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<input type="checkbox"/>	L12	L11 not (L9 or L4)	159
<input type="checkbox"/>	L11	(L1 or L2 or L3) and (dimension or width or overlap\$5).clm.	328
<input type="checkbox"/>	L10	(L1 or L2 or L3) and (dimension or width or overlap\$5)	1117
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<input type="checkbox"/>	L9	L8 and ((width or dimension) with (less or lower or below) with limit)	179
<input type="checkbox"/>	L8	L7 and (limit\$6 same (photolithograph\$2 or lithograph\$2))	3411
<input type="checkbox"/>	L7	L6 and (pattern\$4 same (resist or photoresist))	9430
<input type="checkbox"/>	L6	L5 not L4	27763
<input type="checkbox"/>	L5	((critical adj dimension) or CD or (gate with width) or (line with width)) same (wavelength or photolithograph\$8 or lithograph\$8)	27980
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<input type="checkbox"/>	L4	(L1 or L2 or L3) and ((critical adj dimension) or CD or (gate with width) or (line with width)) and (photolithograph\$8 or lithograph\$8)	437
<input type="checkbox"/>	L3	438/588.ccls.	222
<input type="checkbox"/>	L2	438/587.ccls.	431
<input type="checkbox"/>	L1	438/585.ccls.	1105

END OF SEARCH HISTORY

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Help](#)

Welcome United States Patent and Trademark Office

 [Search Results](#)[BROWSE](#)[SEARCH](#)[IEEE Xplore GUIDE](#) [e-mail](#)

Results for "((gate &lt;and&gt; line &lt;and&gt; width &lt;and&gt; (photolithogpay &lt;or&gt; lithography))&lt;in..."

Your search matched 19 of 1235066 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.» [Search Options](#)[View Session History](#)

## Modify Search

 [»](#)[New Search](#) Check to search only within this results setDisplay Format:  Citation  Citation & Abstract» [Key](#)

IEEE JNL IEEE Journal or Magazine

 Select[Article Information](#)

IEE JNL IEE Journal or Magazine

**1. Patterning sub-30-nm MOSFET gate with I-line lithography**Asano, K.; Yang-Kyu Choi; Tsu-Jae King; Chenming Hu;  
Electron Devices, IEEE Transactions on  
Volume 48, Issue 5, May 2001 Page(s):1004 - 1006  
Digital Object Identifier 10.1109/16.918251[AbstractPlus](#) | [References](#) | [Full Text: PDF\(92 KB\)](#) IEEE JNL**2. A lithography independent gate definition technology for fabricating sub-100 nm devices**Shendong Zhang; Ruqi Han; Xiaoyan Liu; Xudong Guan; Ting Li; Dacheng Zhang;  
Electron Devices Meeting, 2001. Proceedings. 2001 IEEE Hong Kong  
30 June 2001 Page(s):81 - 84  
Digital Object Identifier 10.1109/HKEDM.2001.946923[AbstractPlus](#) | [Full Text: PDF\(584 KB\)](#) IEEE CNF**3. An experimentally validated analytical model for gate line-edge roughness (LER) effects on**Diaz, C.H.; Hun-Jan Tao; Yao-Ching Ku; Yen, A.; Young, K.;  
Electron Device Letters, IEEE  
Volume 22, Issue 6, June 2001 Page(s):287 - 289  
Digital Object Identifier 10.1109/55.924844[AbstractPlus](#) | [References](#) | [Full Text: PDF\(72 KB\)](#) IEEE JNL**4. Experimental investigation of the impact of LWR on sub-100-nm device performance**Hyun-Woo Kim; Ji-Young Lee; Shin, J.; Sang-Gyun Woo; Han-Ku Cho; Joo-Tae Moon;  
Electron Devices, IEEE Transactions on  
Volume 51, Issue 12, Dec. 2004 Page(s):1984 - 1988  
Digital Object Identifier 10.1109/TED.2004.839115[AbstractPlus](#) | [References](#) | [Full Text: PDF\(728 KB\)](#) IEEE JNL**5. Process steps for a double gate MOSFET with vertical layout**Trelkenkamp, St.; Moers, J.; van der Hart, A.; Kordos, P.; Luth, H.;  
Advanced Semiconductor Devices and Microsystems, 2002. The Fourth International Conference on  
14-16 Oct. 2002 Page(s):271 - 274[AbstractPlus](#) | [Full Text: PDF\(247 KB\)](#) IEEE CNF**6. Test chips for evaluating strong phase shift lithography**Ashton, R.A.; Kane, B.C.; Blatchford, J.W.; Shuttleworth, D.M.;  
Microelectronic Test Structures, 2001. ICMTS 2001. Proceedings of the 2001 International Conference on  
14-16 Oct. 2001 Page(s):1 - 4

19-22 March 2001 Page(s):153 - 158

Digital Object Identifier 10.1109/ICMTS.2001.928654

[AbstractPlus](#) | Full Text: [PDF\(420 KB\)](#) IEEE CNF

7. **Fine pattern replication using ETS-1 three-aspherical mirror Imaging system**

Watanabe, T.; Kinoshita, H.; Hamamoto, K.; Okazaki, S.;

Microprocesses and Nanotechnology Conference, 2001 International

31 Oct.-2 Nov. 2001 Page(s):82

Digital Object Identifier 10.1109/IMNC.2001.984089

[AbstractPlus](#) | Full Text: [PDF\(283 KB\)](#) IEEE CNF

8. **Analysis of the impact of proximity correction algorithms on circuit performance**

Li Chen; Milor, L.S.; Ouyang, C.H.; Maly, W.; Yeng-Kuang Peng;

Semiconductor Manufacturing, IEEE Transactions on

Volume 12, Issue 3, Aug. 1999 Page(s):313 - 322

Digital Object Identifier 10.1109/66.778196

[AbstractPlus](#) | References | Full Text: [PDF\(284 KB\)](#) IEEE JNL

9. **19 GHz vertical Si p-channel MOSFET**

Moers, J.; Klaes, D.; Tonnesmann, A.; Vescan, L.; Wickenhauser, S.; Marso, M.; Kordos, P.; Luth, Electronics Letters

Volume 35, Issue 3, 4 Feb. 1999 Page(s):239 - 240

Digital Object Identifier 10.1049/el:19990138

[AbstractPlus](#) | Full Text: [PDF\(228 KB\)](#) IEE JNL

10. **Local flare effects and correction in ArF lithography**

Yao, T.; Osawa, M.; Minami, T.; Yamamoto, N.; Aoyama, H.; Okuda, G.; Sawano, T.; Kamatsuki, I.; Futatsuya, H.; Kobayashi, K.; Ogino, K.; Hoshino, H.; Machida, Y.; Arimoto, H.; Asai, S.; VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on

10-12 June 2003 Page(s):43 - 44

[AbstractPlus](#) | Full Text: [PDF\(258 KB\)](#) IEEE CNF

11. **1D to 1D tunneling in a dual electron waveguide device**

Eugster, C.C.; del Alamo, J.A.; Melloch, M.R.; Rooks, M.J.; Electron Devices, IEEE Transactions on

Volume 40, Issue 11, Nov 1993 Page(s):2135 - 2136

Digital Object Identifier 10.1109/16.239824

[AbstractPlus](#) | Full Text: [PDF\(228 KB\)](#) IEEE JNL

12. **Characterization of SAW devices up to 2.6 GHz on GaAs and InP**

Irby, J.H.; Hunt, W.D.; Corless, R.F.;

Ultrasonics Symposium, 1995. Proceedings., 1995 IEEE

Volume 1, 7-10 Nov. 1995 Page(s):397 - 400 vol.1

Digital Object Identifier 10.1109/ULTSYM.1995.495606

[AbstractPlus](#) | Full Text: [PDF\(348 KB\)](#) IEEE CNF

13. **Record low specific on-resistance for low-voltage trench MOSFETs**

Zandt, M.A.A.; Hijzen, E.A.; Huetting, R.J.E.; Koops, G.E.;

Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G- Circuits, Devices and Systems], Volume 151, Issue 3, 17 June 2004 Page(s):269 - 272

Digital Object Identifier 10.1049/ip-cds:20040444

[AbstractPlus](#) | Full Text: [PDF\(382 KB\)](#) IEE JNL

14. **High speed I<sup>2</sup>L fabricated with electron-beam lithography and ion implantation**

Evans, S.A.; Bartelt, J.L.; Sloan, B.J.; Varnell, G.L.;

1977 International Electron Devices Meeting

Volume 23, 1977 Page(s):266 - 270

[AbstractPlus](#) | Full Text: [PDF\(424 KB\)](#) [IEEE CNF](#)**15. Line-profile and critical dimension measurements using a normal incidence optical metrology**

Weidong Yang; Lowe-Webb, R.; Korlahalli, R.; Zhuang, V.; Sasano, H.; Wei Liu; Mui, D.;

Advanced Semiconductor Manufacturing 2002 IEEE/SEMI Conference and Workshop

30 April-2 May 2002 Page(s):119 - 124

Digital Object Identifier 10.1109/ASMC.2002.1001586

[AbstractPlus](#) | Full Text: [PDF\(664 KB\)](#) [IEEE CNF](#)**16. A 3D sidewall flash EEPROM cell and memory array**

Pein, H.; Plummer, J.D.;

Electron Devices, IEEE Transactions on

Volume 40, Issue 11, Nov 1993 Page(s):2126 - 2127

Digital Object Identifier 10.1109/16.239805

[AbstractPlus](#) | Full Text: [PDF\(228 KB\)](#) [IEEE JNL](#)**17. A fine-line nMOS IC for raster-scan control of a 500-MHz electron-beam deflection system**

Bayruns, R.J.; Suciu, P.I.; Wittwer, N.C.; Fraser, D.L., Jr.; Fuls, E.N.; Kushner, R.A.; Ashley, F.R.; Ger

Electron Devices, IEEE Transactions on

Volume 29, Issue 4, Apr 1982 Page(s):737 - 744

[AbstractPlus](#) | Full Text: [PDF\(1136 KB\)](#) [IEEE JNL](#)**18. A Fine-Line nMOS IC for Raster-Scan Control of a 500-MHz Electron-Beam Deflection System**

Bayruns, R.J.; Suciu, P.I.; Wittwer, N.C.; Fraser, D.L.; Fuls, E.N.; Kushner, R.A.; Ashley, F.R.; Ger

Solid-State Circuits, IEEE Journal of

Volume 17, Issue 2, Apr 1982 Page(s):367 - 374

[AbstractPlus](#) | Full Text: [PDF\(1448 KB\)](#) [IEEE JNL](#)**19. Impact of RSF with variable coefficients for CD variation analysis including OPC**

Goda, A.; Misaka, A.; Odanaka, S.;

Statistical Metrology, 1999. IWSM. 1999 4th International Workshop on

12 June 1999 Page(s):62 - 65

Digital Object Identifier 10.1109/IWSM.1999.773197

[AbstractPlus](#) | Full Text: [PDF\(288 KB\)](#) [IEEE CNF](#)